OPTOELECTRONIC-DEVICE SUBSTRATE, METHOD FOR DRIVING SAME, DIGITALLY-DRIVEN LIQUID-CRYSTAL-DISPLAY, ELECTRONIC APPARATUS, AND PROJECTOR

BACKGROUND OF THE INVENTION

1. Field of Invention

[0001] The present invention relates to an optoelectronic-device substrate, a method for driving this substrate, a digitally-driven liquid-crystal display, an electronic apparatus, and a projector.

2. Description of Related Art

[0002] ~~In general,~~ optoelectronic panels ~~often~~ used for a display have, for example, a liquid-crystal part between a pair of substrates bonded together via a sealing material. These optoelectronic panels have an electrode on one of the surfaces of the substrates, the surfaces facing each other. A voltage according to an image to be displayed is applied on the electrode via routing wiring connected to the electrode.

[0003] In the ~~past~~, a voltage ~~was~~ applied on the liquid-crystal part in an analog fashion. In another case, a voltage ~~was~~ applied on the liquid-crystal part in a digital fashion every one frame or every one sub frame. (Refer to ~~patent reference 1~~, for example.) Further, after a positive effective voltage ~~was~~ applied on the liquid-crystal part, a negative effective voltage with magnitude substantially the same as that of the positive effective voltage ~~was~~ applied so as to prevent electrical charges from being accumulated in liquid-crystal molecules. Subsequently, electrical charges remaining in the liquid-crystal part ~~were~~ cancelled.

~~[0004] [Patent Reference 1]~~

~~[0005]~~ Japanese Unexamined Patent Application Publication No. 2001-100707

SUMMARY OF THE INVENTION

[0006] However, it is difficult to cancel electrical charges completely in the case where a positive voltage and a negative voltage are applied every one frame in the analog fashion or the digital fashion. Therefore, with the passage of time, electrical charges are accumulated in the liquid-crystal part. Subsequently, the liquid-crystal molecules deteriorate.

[0007] Further, the accumulation of the electrical charges becomes the cause of image persistence in the liquid-crystal part.

[0008] The present invention ~~has been achieved for~~ solving the above-described problems and ~~the object thereof is to~~ provide an optoelectronic-device substrate used for a

display panel that can display an image with high quality and high contrast according to a digital driving method, a method for driving this substrate, a digitally-driven liquid-crystal display, an electronic apparatus, and a projector.

[0009] ~~For solving the above-described problems and achieving the above-described object,~~ the present invention provides an optoelectronic-device substrate including a memory-cell array including a plurality of memory cells that is arranged in matrix form and digitally driven and a pixel electrode for retrieving pixel data stored in the memory cells as an electrical signal. In this case, each of the memory cells has a phase-inversion circuit for inverting the phase of transmitted pixel data, or a data-inversion signal whose phase is inverted by the phase-inversion circuit is transmitted to the pixel electrode. Subsequently, it becomes possible to cancel an electrical charge remaining in a liquid-crystal layer or the like in the memory cell. Further, it becomes possible to display an image with high quality and high contrast through the digital-driving method.

[0010] Further, according to a preferred mode of the present invention, each of the memory cells ~~comprises~~ includes a storage unit for storing the pixel data, a first analog switch for generating the data-inversion signal, based on the phase-inversion signal, and a second analog switch for switching between the data-inversion signal from the first analog switch and a zero-data signal. The data-inversion signal may preferably be selected when the pixel data is stored in the storage unit and the zero-data signal may preferably be selected when the pixel data is not stored in the storage unit. Therefore, since the memory cell has the data-inversion function, the driving capability of a phase-inversion-signal shift driver that ~~will be~~ described ~~later~~ below can be reduced.

[0011] Further, according to another preferred mode of the present invention, the storage unit may preferably be formed as an SRAM. Subsequently, it becomes possible to reliably hold data in a digital fashion.

[0012] Further, according to another preferred mode of the present invention, the memory-cell array may preferably ~~comprise~~ include a plurality of first signal lines for connecting one group of address terminals included in one group of the memory cells in parallel, the one group of the memory cells being provided along a row direction, a plurality of second signal lines for connecting one group of data terminals included in one group of the memory cells in parallel, the one group of the memory cells being provided along a column direction, and a plurality of third signal lines for connecting one group of phase-inversion terminals included in one group of the memory cells in parallel, the one group of the memory cells being

provided along the row direction or the column direction. Further, the optoelectronic-device substrate may preferably further comprise a first driver circuit for transmitting address signals in sequence to the memory cells via the plurality of first signal lines, the memory cells being provided along the row direction, a second driver circuit for transmitting the pixel data to the memory cells at one time via the plurality of second signal lines, the memory cells being provided along the column direction, and a third driver circuit for transmitting phase-inversion signals to each group of the memory cells via the plurality of third signal lines, the group of the memory cells being provided along the row direction or the column direction. Accordingly, it becomes possible to store two-dimensional data, such as image data, in the plurality of memory cells.

[0013] Further, according to another preferred mode of the present invention, the third driver circuit has a phase-inversion circuit for inverting the phase of the pixel data and the phase-inversion circuit inverts the phase of the pixel data before the pixel data is transmitted to the memory cells. Subsequently, it becomes possible to reduce the number of transistors forming each memory cell, whereby the size of each pixel is reduced.

[0014] Further, according to another preferred mode of the present invention, the memory-cell array comprises a plurality of first signal lines for connecting one group of address terminals included in one group of the memory cells in parallel, the one group of the memory cells being provided along a row direction, a plurality of second signal lines for connecting one group of data terminals included in one group of the memory cells in parallel, the one group of the memory cells being provided along a column direction, and a plurality of third signal lines for connecting one group of phase-inversion terminals included in one group of the memory cells in parallel, the one group of the memory cells being provided along the row direction or the column direction. The optoelectronic-device substrate may further comprise a row-address-decoder driver circuit for transmitting row-address data for selecting any of rows of the memory cells via the plurality of first signal lines, the memory cells being provided along the row direction, a column-address-decoder driver circuit for transmitting column-address data for selecting any of columns of the memory cells via the plurality of second signal lines, the memory cells being provided along the column direction, and the pixel data output to the memory cells designated by the row-address data and the column-address data, and a phase-inversion driver circuit for transmitting a phase-inversion signal to each group of the memory cells via the plurality of third signal lines, the each group of the memory cells being provided along the row direction or the column direction. According to this configuration, it becomes possible to select a predetermined memory cell at the

intersection of any row and any column by using the row-address data for selecting any of rows of the memory cells and the column-address data for selecting any of columns of the memory cells. Further, it becomes possible to rewrite the pixel data of the selected arbitrary memory cell on a random basis, irrespective of the arrangement of the memory cells. As a result, it becomes unnecessary to transfer pixel data to be displayed to the memory cells whose pixel data need not to be rewritten. Subsequently, the power consumption required for the data-rewriting operation decreases. Consequently, it becomes possible to reduce the power consumption required for an image-display device, such as a digitally-driven liquid-crystal display, an electronic apparatus, a projector, and so forth, the image-display device using the above-described optoelectronic-device substrate.

[0015] Further, according to another preferred mode of the present invention, the phase-inversion driver circuit has a phase-inversion circuit for inverting the phase of the pixel data. The phase-inversion driver circuit may preferably invert the phase of the pixel data in a predetermined cycle regardless of the number of the memory cells whose display information is rewritten according to the pixel data. For example, in the case of a liquid-crystal display including the optoelectronic-device substrate is used, it becomes possible to perform operations for refreshing display data applied on a liquid-crystal layer of the liquid-crystal display. That is to say, it becomes possible to perform the refreshing operation (phase-inversion process) with cycles according to the liquid-crystal performance regardless of whether or not the pixel data to be displayed is changed. In the case where the liquid-crystal display displays a still image, the refreshing operation (the phase-inversion operation), which is necessary for displaying a moving image, can be omitted. Subsequently, it becomes possible to prevent image persistence on the liquid crystal by performing a minimum of the refreshing operation according to the performance of the liquid crystal. Consequently, it becomes possible to reduce the power requirements of an image-display device, such as a digitally-driven liquid-crystal display, an electronic apparatus, a projector, and so forth, the image-display device using the above-described optoelectronic-device substrate.

[0016] Further, the present invention provides an electronic apparatus having the above-described optoelectronic-device substrate and a display unit for displaying an image through the optoelectronic-device substrate. Subsequently, it becomes possible to display an image with high quality and high contrast.

[0017] The present invention provides a projector having a light-source unit for supplying illumination light, the above-described optoelectronic-device substrate, a display

unit ~~for~~ displaying an image by using the optoelectronic-device substrate, and a projection-lens system ~~for~~ projecting the image of the display unit. Subsequently, it becomes possible to project an image with high quality and high contrast.

[0018] According to another preferred mode of the present invention, a method ~~for~~ driving an optoelectronic-device substrate ~~comprising~~ a memory-cell array including a plurality of memory cells that is arranged in matrix form along a row direction and a column direction and that is digitally driven preferably ~~comprises~~ a phase-inversion process ~~for~~ inverting the phase of the pixel data transmitted to the memory cells. Subsequently, electrical charges remaining in, for example, a liquid-crystal layer in the memory cell can be cancelled. Further, it becomes possible to display an image with high quality and high contrast by using the digital-driving method.

[0019] Further, according to preferred mode of the present invention, in the phase-~~inversion process~~, the pixel data is subjected to pulse-width modulation, one frame is divided into a plurality of sub-frames, and the phase of the display data in the sub-frames is preferably shifted to the plus side to the minus side with about one-half cycles. Subsequently, it becomes possible to cancel an electrical charge ~~for~~ reducing deterioration of liquid-crystal molecules in a liquid-crystal display panel, for example. Accordingly, image persistence in the liquid-crystal part can be prevented.

[0020] According to another preferred mode of the present invention, in the phase-inversion process, the memory cells provided along the row direction are preferably selected in sequence and the phase of the pixel data is inverted at the same time. Subsequently, it becomes possible to efficiently perform sub-frame rewriting without wasting time.

[0021] According to another preferred mode of the present invention, the phase-inversion process includes sub-frame-cycle varying process ~~for~~ making a cycle of the sub-frames variable through changing a cycle with which the phase-inversion signal is transmitted to the memory cells provided along the row direction and a cycle with which the pixel data is transmitted to the memory cells provided along the row direction. Subsequently, it becomes possible to arbitrarily change the cycle of the sub-frames.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Fig. 1 shows ~~the schematic configuration of~~ a reflection liquid-crystal display panel according to a first embodiment of the present invention;

[0023] Fig. 2 shows ~~the schematic configuration of~~ an optoelectronic-device substrate according to the first embodiment;

[0024] Figs. 3(A) and 3(B) show the configuration of a memory cell according to the first embodiment;

[0025] Fig. 4 illustrates a voltage applied to a liquid-crystal layer;

[0026] Figs. 5(A) and 5(B) illustrate a sub-frame driving method;

[0027] Figs. 6(A), 6(B), and 6(C) illustrate PWM;

[0028] Fig. 7 shows the schematic configuration of an example modification of the optoelectronic-device substrate according to the first embodiment;

[0029] Fig. 8 shows the schematic configuration of a row driver according to the first embodiment;

[0030] Fig. 9 shows the schematic configuration of a column driver according to the first embodiment;

[0031] Fig. 10 is a timing chart of the column driver according to the first embodiment;

[0032] Fig. 11 is a timing chart of the row driver according to the first embodiment;

[0033] Fig. 12 is a timing chart relating to data transmission according to the first embodiment;

[0034] Fig. 13 is a timing chart illustrating the relationship between the row driver and the column driver according to the first embodiment;

[0035] Fig. 14 shows the schematic configuration of a phase-inversion-signal shift driver according to the first embodiment;

[0036] Fig. 15 is a timing chart of the phase-inversion-signal shift driver according to the first embodiment;

[0037] Fig. 16 is a timing chart illustrating how sub-frames according to the first embodiment are displayed in sequence;

[0038] Figs. 17(A) and 17(B) illustrate the configuration of a memory cell according to a second embodiment of the present invention;

[0039] Fig. 18 shows the schematic configuration of an optoelectronic-device substrate according to a third embodiment of the present invention;

[0040] Fig. 19 shows the schematic configuration of a projector according to a fifth embodiment of the present invention;

[0041] Figs. 20(A), 20(B), and 20(C) are external views of electronic apparatuses according to a sixth embodiment of the present invention;

[0042] Fig. 21 shows ~~the schematic configuration of~~ an optoelectronic-device substrate according to a fourth embodiment of the present invention;

[0043] Fig. 22 shows ~~the schematic configuration of~~ a phase-inversion-signal driver according to the fourth embodiment.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0044] ~~Preferred~~ embodiments of the present invention ~~will now be~~ described in detail with reference to the attached drawings.

[0045] (First Embodiment)

[0046] (Reflection liquid-crystal display panel)

[0047] Fig. 1 is a sectional view of a reflection liquid-crystal display panel 10 including an optoelectronic-device substrate according to a first embodiment of the present invention. A circuit-forming layer 12 including pixel electrodes 17 is formed on a silicon substrate 11. The pixel electrodes 17 are arranged in matrix form. A transparent substrate 14 is provided so as to face the silicon substrate 11. An liquid-crystal layer 15 is formed between the silicon substrate 11 and the transparent substrate 14. The liquid-crystal layer 15 is sealed by a sealing material 13.

[0048] A counter COM electrode 16 is formed on the silicon-substrate-11 side of the transparent substrate 14. A terminal pad 19 is provided on one end of the silicon substrate 11. A flexible-tape wiring 21 is bonded to the terminal pad 19 by using an anisotropic conductive adhesive 20.

[0049] The elements of the reflection liquid-crystal display panel 10 are all formed on the circuit-forming layer 12 on the silicon substrate 11. A driving circuit for driving the pixel electrodes 17, and a row driver, a column driver, and a phase-inversion-signal shift driver that are provided near the substrate are formed near and around the pixels on the same substrate.

[0050] The reflection liquid-crystal display panel 10 has two main characteristics. One of the two main characteristics is that a voltage is applied to the liquid-crystal layer 15 in a digital fashion and a pair of voltages inverted to each other, that is, a positive voltage and a negative voltage, is applied to the liquid-crystal layer 15 in one frame (or one sub-frame that ~~will be~~ described ~~later~~). The other of the two main characteristics is that a sub-frame driving method described ~~later~~ is used for displaying an image and rewriting is performed for each of lines for displaying the lines in sequence. These characteristics ~~will be~~ described ~~later~~ in detail.

[0051] (Schematic configuration of Optoelectronic-device substrate)

[0052] Fig. 2 is a block diagram illustrating the inner configuration of the circuit-forming layer 12 including the driving circuit and the above-described drivers. The circuit-forming layer 12 has a memory-cell array (a digital storage) 140, a row driver 110, a column driver 120, and a phase-inversion-signal shift driver 130. Signals DY, DATA, and DFC are transmitted from a control circuit (not shown) to the drivers 110, 120, and 130, respectively. Further, clock signals CLY, #CLY, CLX, #CLX, CLFC, #CLFC are transmitted from the control circuit to the drivers 110, 120, and 130, respectively.

[0053] ~~In this specification, signals having symbol # at the top of their reference characters correspond to signals having a bar on their reference characters, the signals being shown in the drawing.~~ The logic levels of signals having ~~neither symbols # nor~~ bars and those ~~of the signals~~ having ~~symbols # or~~ bars are inverted to one another.

[0054] The memory-cell array 140 includes a plurality of memory cells 101 that is arranged in two-dimensional matrix form (array form) and can store image data corresponding to one screen. Each of the memory cells 101 includes a pair of data terminals 102d1 and 102d2, an address terminal 102a, a phase-inversion terminal 102f, and an output terminal (not shown).

[0055] The memory-cell array 140 includes a plurality of address lines (first signal lines) 111 that are electrically connected to the row driver (a first driver circuit) 110, a plurality of a pair of data lines (second signal lines) 120a and 120b that is electrically connected to the column driver (a second driver circuit) 120, and a plurality of phase-inversion-signal lines (third signal lines) 131 that is electrically connected to the phase-inversion-signal shift driver (a third driver circuit) 130.

[0056] The address lines 111 connect the address terminals 102a of the plurality of memory cells in parallel, the memory cells being arranged along the row direction (a first direction). The data lines 120a connect the data terminals 102d1 of the plurality of memory cells in parallel, the memory cells being arranged along the column direction (a second direction orthogonal to the first direction). Similarly, the data lines 120b connect the data terminals 102d2 of the memory cells in parallel, the memory cells being arranged along the column direction. The phase-inversion-signal lines 131 connect the phase-inversion terminals 102f of the plurality of memory cells in parallel, the memory cells being arranged along the row direction (the first direction).

[0057] (The configuration of Memory cell)

[0058] Fig. 3(A) shows the schematic configuration of the memory cell 101. The memory cell 101 has a storage unit 200 and two analog switches SW1 and SW2. The storage unit 200 is formed as an SRAM for storing image-data signals DATA and $\overline{DATA}$ that are transmitted from ends Dn and $\overline{Dn}$ of the column driver 120. The first analog switch SW1 transmits a data-inversion potential Dout to the second analog switch SW2, based on a phase-inversion signal FC. The second analog switch SW2 transmits either the data-inversion potential Dout transmitted from the first analog switch SW1 or a reference potential COM to the pixel electrode 14 according to the data stored in the storage unit 200. The reference potential COM is equivalent to a potential given to the counter COM electrode 16 shown in Fig. 1. In the case where the storage unit 200 stores the image-data signal DATA, the data-inversion potential Dout is given to the pixel electrode 14. Therefore, a voltage obtained by subtracting the data-inversion potential from the reference potential COM is applied to the liquid-crystal layer 15. In the case where the storage unit 200 does not store the image-data signal DATA, the reference potential COM is given to the pixel electrode 14, whereby the difference between the potential of the pixel electrode and that of a common electrode becomes zero. In this case, no voltage is applied to the liquid-crystal layer 15.

[0059] Fig. 3(B) illustrates transistors of the memory cell 101 for describing the configuration of the memory cell 101. Transistors T1 to T6 correspond to the storage unit 200. Transistors T7 to T10 correspond to the analog switch SW2, and transistors T11 to T12 correspond to the analog switch SW1, respectively. Since the analog switch SW1 is formed in the pixel, the driving capability of an FC line can be reduced.

[0060] Since the memory cell 101 has a memory formed as an SRAM, the column driver 120 transmits a signal $\overline{Dj}$ (reference character j is an integer from 0 to m. Reference character m is the column number of the pixel array.) to the memory-cell array 140. Although a signal Dj may be given to the memory-cell array 140, in the case where the signals Dj and $\overline{Dj}$ are given to the memory-cell array 140, the speed of data determination increases. Therefore, the signals Dj and $\overline{Dj}$ may preferably be given to the memory-cell array 140. The memory of the memory-cell array 140 may be formed as a memory that does not require the signal $\overline{Dj}$. In this case, the column driver 120 may not output the signal $\overline{Dj}$ to the memory-cell array 140. However, in this embodiment, the memory in the memory-cell array 140 should be formed as an SRAM memory for at least the following two reasons. First, since the configuration of the SRAM memory is simple, it is easy to provide the SRAM

memory for each pixel area of a spatial light modulator. Second, since the SRAM memory can operate at high speed, it is suitable for image-data processing.

[0061] (Voltage applied to Liquid-crystal layer)

[0062] Fig. 4 illustrates a voltage applied to the liquid-crystal layer 15. The main object of providing Fig. 4 is to illustrate the applied voltage. The applied voltage is one of the characteristics of the present invention. The operations of the drivers 110, 120, and 130 will be described later in detail. Further, the sub-frame will be described later. First, an address signal Yi (Reference character i is an integer from 1 to n. Reference character n is the row number of the pixel array.) from the row driver 110 is transmitted to the memory cell 101 provided along the row direction. A phase-inversion signal FCi (The reference character i is an integer from 1 to n.) from the phase-inversion-signal shift driver 130 is shifted from H level to L level, or vice versa, with one-half cycles within the sub-frame. Further, the data signal Dj of the column driver 120 is transmitted according to the address signal Yi from the row driver 110.

[0063] As shown in Fig. 3(A), the first analog switch SW1 generates a data-inversion potential Douti, based on the phase-inversion signal FCi. Further, the second analog switch SW2 switches between the data-inversion potential Douti transmitted from the first analog switch SW1 and the reference potential COM. Therefore, in a frame to which the data signal Di of the column driver 120 is input, a voltage is applied to the liquid-crystal layer 15. In this case, a potential given to the pixel electrode is switched between a potential Vcc and a potential GND with one-half cycles in the sub frame. The difference between the reference potential COM and the potential Vcc is equivalent to the difference between the reference potential COM and the potential GND. Therefore, a voltage that has a phase opposite to those of effective voltages Va and Vb with reference to the reference voltage COM and that has a magnitude equivalent to those of the effective voltages Va and Vb is applied to the liquid-crystal layer 15.

[0064] The liquid-crystal layer 15 performs a predetermined operation without being affected by applied voltages so long as the magnitude of the applied voltages (the effective voltages) is identical. The operation of the liquid-crystal layer 15 does not change according to whether the phase of each applied voltage is positive or negative. Further, positive voltages and negative voltages in equal proportions are applied to the liquid-crystal layer 15 in a digital fashion for producing an image display corresponding to one frame. In this case, the magnitude of each positive voltage is equivalent to that of each negative

voltage. Therefore, no electrical charges remain in liquid-crystal molecules. That is to say, almost all the electrical charges are cancelled. Consequently, the electrical charges remaining in the liquid-crystal layer 15 for long time are reduced, whereby image persistence is prevented.

[0065] (Sub-frame driving method)

[0066] The principle of a sub-frame driving method ~~will now be~~ described. In the past, a voltage corresponding to the gray scale of an image was applied to the liquid-crystal layer in an analog fashion. The gray scale can be presented according to the magnitude of the applied voltage. However, in the case of the reflection liquid-crystal display panel 10 according to this embodiment, on voltages and off voltages are applied to the liquid-crystal layer 15 in the digital fashion as described above. In this case, therefore, it is impossible to present the gray scale of the image according to the magnitude of the applied voltages as in the past. Therefore, the gray scale of the image is presented according to the sub-frame driving method using pulse-width modulation (hereinafter ~~referred to as~~ "PWM").

[0067] First, the sub-frame driving method ~~will be~~ described. For the sake of simplicity, the image is presented with eight levels of gray (three bits). In this case, one frame includes three sub-frames, that is, first to third sub-frames 1SF to 3SF.

[0068] Fig. 5(A) illustrates the arrangement of the pixels. As shown in this drawing, an image corresponding to one frame is formed by pixels of 1024 rows. The one frame includes first to n-th lines. One sub-frame includes an address period Ta for writing data to a memory cell and a display period for displaying the image according to the written data. In one sub-frame period, the image-data signal DATA is stored in each memory cell (a pixel) so as to be turned on when the sub-frame has a weight required for displaying the frame. A method for assigning the weight to the sub-frame will be described later in a description of the PWD. A time period where the image-data signal DATA is displayed corresponds to a lit state. Fig. 5(B) illustrates the relationship between one frame and sub-frames. The one frame includes the three sub-frames 1SF to 3SF. Address periods Ta of the sub-frames are all the same with one another. However, display periods of the sub-frames are different from one another. The number of the sub-frames increases and decreases according to the number of gray levels of an image to be displayed. A sub-frame corresponding to an image that is displayed for long time such as the sub-frame 3SF may preferably be divided. Consequently, spurious profiles are reduced, whereby the quality of the displayed image increases.

[0069] (PWM)

The PWM will now be described with reference to Fig. 6. First, an example where an image is presented with sixteen gray levels (four bits) will be described. In this case, as shown in Fig. 6(A), four sub-frame pulses P0 (=20), P1 (=21), P2 (=22), and P3 (=23) are used, the four sub-frame pulses having weights corresponding to the bits or presenting the four-bit gray scale, respectively. Fig. 6(B) illustrates the timing chart of the sub-frame pulses P0, P1, P2, and P3. As shown in Fig. 6(C), in the case where an image is presented with ten levels of gray, for example, the memory cell is lit in synchronization with the sub-frame pulses P1 and P3 in the one-frame display period. Consequently, the integral of the lit time in the one frame corresponds to the gray scale of the actual image to be displayed. Similarly, when the gray level of the image is changed from ten to six, the memory cell is lit in synchronization with the sub-frame pulses P1 and P2. As has been described, in the case of the reflection liquid-crystal-display panel of this embodiment, the gray scale of an image to be displayed is presented according to the above-described sub-frame driving method and the above-described PWM method.

[0070] (Example modification of Optoelectronic-device substrate)

[0071] The principle of characteristic arts of the present invention, the characteristic arts being used for the optoelectronic-device substrate shown in Fig. 2, has been described. For adjusting periods for rewriting the data signal DATA so that the rewriting periods become equal to one another, AND circuits and a signal WE may be used as shown in Fig. 7. The difference between the configuration shown in this drawing and that shown in Fig. 2 is that the AND circuits for the address signals Y transmitted from the row driver and the signal WE are added. The rest of the configuration shown in Fig. 7 is the same as that shown in Fig. 2. Therefore, the same parts are indicated by the same reference numerals and the description thereof is omitted.

[0072] The configuration and function of each driver will now be described with reference to the configuration shown in Fig. 7.

[0073] (The configuration of Row driver)

[0074] Fig. 8 is a block diagram illustrating an example configuration of the row driver 110. The row driver 110 transmits address signals (scan signals) Yi in sequence, from upper downward in the case of Fig. 7, to each group of the memory cells via the address lines 111, the group of memory cells being provided along the row direction.

[0075] The row driver 110 comprises a shift-register circuit 110a having a plurality of registers including three inverters and an AND-logic circuit 110b having a plurality of

AND gates. The shift-register circuit 110a has the serial-parallel-conversion function. An address signal DY in pulse form is transmitted to a first register and transferred to a second register and beyond according to the clock signals CLY and #CLY. Further, the address signal DY is output from the registers. The AND gates of the AND-logic circuit 110b output the logical conjunction of data transmitted from two registers adjacent to each other as the address signal Yi or the like. Subsequently, the AND-logic circuit 110b outputs the address signal Yi with relatively high time resolution, that is, the address signal Yi that is shifted to H level only for a short period of time during which the address signal DY is shifted by the clock signals CLY and #CLY (the one-half cycle of the clock signals CLY and #CLY).

[0076] (The Configuration of Column driver)

[0077] Fig. 9 is a ~~block diagram~~ illustrating an example configuration of the column driver 120. The column driver 120 transmits the pairs of data signals D and #D to the groups of the memory cells at the same time via the pairs of data lines 120a and 120b, the memory-cell groups being provided along the column direction. The column driver 120 ~~comprises~~ includes a shift-register circuit 120a including a plurality of registers having six inverters. The shift-register circuit 120a has the serial-parallel-conversion function. The image-data signal DATA is transmitted to the first register and transferred to the second register and beyond. Further, the image-data signal DATA is output from each register. A pair of signals Q and #Q that are output corresponds to the signals D and #D shown in Fig. 7.

[0078] (Timing chart of Column driver)

[0079] Fig. 10 shows a timing chart illustrating the operation of the column driver 120. As shown in this drawing, each register including the six inverters transfers data in sequence at the falling edge of the clock signal CL.

[0080] As described above, when the enable signal WE is at an H level, the address signals Y at the H level are transmitted to the memory cells on a predetermined row to which the data signals D and #D should be transmitted.

[0081] Subsequently, each memory cell 101 can store data in the state where no crosstalk or the like is generated.

[0082] (Timing chart of Row driver)

[0083] Fig. 11 illustrates a timing chart illustrating the operation of the row driver 110. At time t1, the address signal DY indicating that the time period of the first sub-frame 1SF is started is transmitted from the control circuit (not shown) to the row driver 110. The row driver 110 transmits the shifted address signals Yi to the memory cells 101 on each row

in sequence via the plurality of address lines 111 based on the address signal DY. For example, at time t2, the address signal Y0 is transmitted to the memory cells 101 on the first row via the first address line 111. The memory cells on the first line latch the data signals D and $\overline{D}$ transmitted via the pairs of data lines 120a and 120b at the falling edge of the address signal Y0, that is, at the rise of a signal WY0. Fig. 12 shows a timing chart illustrating the timing of transmitting the image-data signals DATA according to the clock signals CLX in the row direction.

[0084] (Timing chart relating to Row and Column)

[0085] Fig. 13 is a timing chart illustrating the relationship between the address signals DY on a predetermined row and the timing of writing the data signals DATA. For example, in the first sub-frame 1SF, a predetermined row is selected by the address signal Y1 and the image-data signals DATA along the column direction are written into the memory cells 101 at the same time.

[0086] (The configuration of Phase-inversion-signal shift driver)

[0087] Fig. 14 illustrates the schematic configuration of the phase-inversion-signal shift driver 130. The phase-inversion-signal shift driver 130 comprises a shift-register circuit 130a including a plurality of registers having three inverters and an AND-logic circuit 130b including a plurality of AND gates. The shift-register circuit 130a has the serial-parallel conversion function. A phase-inversion signal DFC in pulse form transmitted to the first register is transferred to the second register and beyond according to the clock signals CLFC and $\overline{CLFC}$ and output from each register. Each of the AND gates of the AND-logic circuit 130b outputs the logical conjunction of the data transmitted from the two adjacent registers as the phase-inversion signal FC0 or the like.

[0088] (Timing chart relating to Phase-inversion-signal shift driver)

[0089] Fig. 15 shows a timing chart of the phase-inversion-signal shift driver. A comparison of the configuration of the row driver 110 (shown in Fig. 8) and that of the phase-inversion-signal shift driver 130 (shown in Fig. 14) clearly shows that the configuration of the row driver 110 and that of the phase-inversion-signal shift driver 130 are the same with each other. Therefore, the operation shown by the timing chart of Fig. 15 and the operation performed by the row driver 110 shown by the timing chart of Fig. 11 are identical with each other. Here, since a signal Ym0 or greater and a phase-inversion signal FCm0 or greater that are output from the shift registers correspond to the identical operations, respectively, the description thereof will be omitted.

[0090] (Timing chart relating to Image display)

[0091] Fig. 16 shows a timing chart relating to operations performed for displaying an image in the case where an optoelectronic-circuit substrate 100 is used. In this drawing, the phase-inversion signal FC0 and beyond are shifted in sequence according to the address signal Yi and beyond. For example, if the time period of the second sub-frame 2SF starts on the first row, an image corresponding to the first sub-frame 1SF is displayed on the second row and beyond. According to this image-display method, it becomes possible to write continuously in the sub-frames without wasting time. The cycle of the signal DFC can be changed by changing the incidence of the signal DY even though the incidence of the clock signal CLY (CLFC) is not changed.

[0092] (Second Embodiment)

[0093] Fig. 17(a) illustrates the schematic configuration of a memory cell 400 of an optoelectronic-device substrate according to a second embodiment of the present invention. The difference between the memory cell 101 of the first embodiment and the memory cell 400 of this embodiment is that the memory cell 101 has the two analog switches SW1 and SW2 while the memory cell 400 has the analog switch SW2 alone. The other configuration of the memory cell 400 is the same as that of the first embodiment, the same parts will be designated by the same reference numerals and the description thereof will be omitted. Further, since the configuration of the optoelectronic-device substrate is the same as that shown in Fig. 2, the description thereof will be omitted. In this embodiment, the phase-inversion-signal shift driver 130 has the function of generating a data-inversion potential, based on the phase-inversion signal FC.

[0094] Fig. 17(b) shows the configuration of the memory cell 400 by illustrating the transistors thereof. Transistors T1 to T6 correspond to a storage unit 401 and transistors T7 to T10 correspond to the analog switch SW2. Thus, since the phase-inversion-signal shift driver 130 functions as the analog switch SW1, the number of transistors forming the pixel can be reduced. Consequently, the pixel size can be reduced.

[0095] (Third Embodiment)

[0096] Fig. 18 shows the schematic configuration of an optoelectronic-device substrate according to a third embodiment of the present invention. This embodiment is different from the first embodiment in that two partial-column drivers 500a and 500b are provided. Since the other configuration is the same as that of the first embodiment, the same

parts are designated by the same reference numerals and the description thereof ~~will be~~ is omitted.

[0097] Since the above-described two partial-column drivers 500a and 500b are provided, it becomes possible to transmit data in parallel to the memory cells and reduce the quantity of data subjected to the serial-parallel conversion performed by the partial-column drivers. Subsequently, it becomes possible to display an image with high speed even though a large number of pixels are provided. Further, the number of the partial-column driver is not limited to two but can be three or more. Three partial-column drivers or more can handle pixels more than those in the above-described exemplary embodiments.

[0098] (Fourth Exemplary Embodiment)

[0099] Fig. 21 illustrates the schematic configuration of an optoelectronic-device substrate according to a fourth exemplary embodiment of the present invention. This exemplary embodiment is different from the first exemplary embodiment in that a column-address decoder driver 1320 is provided in place of the column driver 120, a row-address decoder driver 1310 in place of the row driver 110, and a phase-inversion-signal driver 1330 in place of the phase-inversion-signal shift driver 130. Since the other configuration of this optoelectronic-device substrate is the same as that of the first exemplary embodiment, the same parts are designated by the same reference numeral and the description thereof is omitted.

[0100] A predetermined memory cell at an arbitrary address can be specified and selected by using row-address data RAD and column-address data CAD. The column-address decoder driver 1320 outputs pixel data that is to be stored in the selected address memory cell 101 from the data lines (the second signal lines) 120a and 120b.

[0101] For example, a method ~~for~~ of rewriting pixel data stored in a diagonally-shaded memory cell 101P, the memory cell 101P being one of the plurality of memory cells 101 shown in Fig. 21, ~~will now be~~ is considered below. In this case, the row-address data RAD ~~for~~ to selecting the address signal Y1 that is output is transmitted to the row-address decoder driver 1310. Further, the column-address data CAD for selecting an output D1 and pixel data to be written in the memory cell 101P are transmitted to a display-data terminal of the column-address decoder driver 1320 at the same time. In this manner, it becomes possible to rewrite the pixel data stored in the memory cell 101P that is arbitrarily selected from among the plurality of memory cells 101 on a random basis, irrespective of the arrangement of the memory cells 101. As a result, it becomes unnecessary to transfer pixel data to be displayed

to memory cells 101 whose pixel data to be displayed needs not be rewritten. Subsequently, the power consumption required for the data-rewriting operation decreases.

[0102] Fig. 22 shows the schematic configuration of the phase-inversion-signal driver 1330. The phase-inversion-signal driver 1330 includes a plurality of buffer amplifiers 1340. Each buffer amplifier 1340 amplifies and generates a data-inversion potential according to the phase-inversion signal DFC (the data-inversion potential corresponding to the Vcc or GND potential shown in Fig. 3). The phase-inversion-signal driver 1330 transmits the generated data-inversion potential from outputs FC0 to FCn to all the memory cells 101. Subsequently, it becomes possible to invert the phase of the potential of a voltage applied on the liquid crystal, the voltage being output from the pixel electrode, regardless of all the quantity of rewriting the memory cells 101, that is, the number of memory cells 101 to be rewritten. Therefore, it becomes possible to perform operations for refreshing display data applied on the liquid-crystal layer 15 (shown in Fig. 1). That is to say, it becomes possible to perform the phase-inversion process with cycles according to the liquid-crystal performance regardless of whether or not the display data is changed. Consequently, it becomes possible to prevent the image persistence on the liquid crystal by performing a minimum of the refreshing operations according to the performance of the liquid crystal. Further, it becomes possible to reduce the power requirements of an image-display device, such as a digitally-driven liquid-crystal display, an electronic apparatus, a projector, and so forth, the image-display device using the above-described optoelectronic-device substrate 1300.

[0103] (Fifth Embodiment)

[0104] Fig. 19 illustrates the schematic configuration of a projector 600 according to a fifth embodiment of the present invention. The projector 600 has a main unit 610 and a projection-lens system 620. The main unit 610 has a light-source unit 611 for supplying light, a digitally-driven liquid-crystal display 613 including the optoelectronic-device substrate according to the above-described embodiments, and a control circuit 612 for controlling the digitally-driven liquid-crystal display 613. The projection-lens system 620 magnifies an image displayed on the digitally-driven liquid-crystal display 613 and projects the magnified image onto a screen 630. Since the projector 600 has the optoelectronic-device substrate according to the above-described embodiments, it becomes possible to project an image with high quality and high contrast according to a digital-driving method. Further, the power requirements of the projector 600 can be reduced.

[0105] (Sixth Embodiment)

[0106] Figs. 20(A), 20(B), and 20(C) show example electronic apparatuses according to a sixth exemplary embodiment of the present invention, respectively. Fig. 20(A) is a perspective view of a mobile phone 1000. The mobile phone 1000 has a liquid-crystal display 1001 using the optoelectronic-device substrate of the present invention. Fig. 20(B) is a perspective view of a wristwatch-type electronic apparatus 1100. The wristwatch-type electronic apparatus 1100 has a liquid-crystal device 1101 using the optoelectronic-device substrate of the present invention. Fig. 20(C) is a perspective view of an example mobile information-processing apparatus 1200 such as a word processor, a personal computer, and so forth. The mobile information-processing apparatus 1200 has an input unit 1202 such as a keyboard or the like, an information-processing device 1204, and a liquid-crystal display 1206 using the optoelectronic-device substrate of the present invention. Since each of these electronic apparatuses includes the optoelectronic-device substrate according to the above-described exemplary embodiments, it becomes possible to obtain an image with high quality and high contrast according to the digital-driving method. Further, the power requirements of these electronic apparatuses can be reduced. The present invention is not limited to the above-described exemplary embodiments but can be modified in various ways within the scope of the spirit thereof.